

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-4 (Canceled)

5. (Original) A semiconductor device, comprising:

a first step structure portion formed at a predetermined level from a surface of a reference layer;

second step structure portions respectively formed on said first step structure portion and said reference layer and functioning as non-LOCOS insulating device isolation blocks for demarcating an element active region on said reference layer; and

a first conductive film patterned on said element active region across at least said second step structure portion on said reference layer,

wherein an upper surface of said first conductive film is planarized such that said upper surface of said first conductive film and an upper surface of said second step structure portion formed on said first step structure portion are formed at substantially the same level.

6. (Original) A device according to claim 5, wherein said upper surface of said first conductive film and said upper surfaces of said second step structure portions are planarized by chemical mechanical polishing.

7. (Original) A device according to claim 5, wherein said reference layer is a semiconductor substrate.

8. (Original) A device according to claim 5, wherein said first step structure portion is a first insulating film formed on a scribing line region of said semiconductor substrate.

9. (Original) A device according to claim 5, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a shield plate electrode buried in an insulating layer.

10. (Original) A device according to claim 5, wherein said first conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said first conductive film.

11. (Original) A device according to claim 5, wherein said first conductive film is a gate electrode.

12. (Original) A device according to claim 5, wherein said reference layer is a semiconductor substrate in which a groove portion is formed, a portion of said semiconductor substrate surrounding the groove portion serves as said first step structure portion, and an element region is formed in the groove portion.

13. (Original) A device according to claim 12, wherein said first step structure portion is an insulating film formed on a scribing line region of said semiconductor substrate.

14. (Original) A device according to claim 12, wherein said second step structure portion is a non-LOCOS insulating device isolation block for demarcating said element active region on an element region.

15. (Original) A device according to claim 14, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a shield plate electrode buried in an insulating layer.

16. (Original) A device according to claim 12, wherein said first conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said first conductive film.

17. (Original) A device according to claim 12, wherein said first conductive film is a gate electrode.

18. (Original) A device according to claim 5, wherein said reference layer is an insulating interlayer stacked on said semiconductor substrate, first wiring layers are formed in said first and second step structure portions, and said first conductive film functions as a second wiring layer.

19. (Original) A device according to claim 18, further comprising another insulating interlayer having a contact hole and formed under said insulating interlayer, and a memory capacitor patterned on said another insulating interlayer, in which a storage node electrode, a dielectric film, and a cell plate electrode having planarized surfaces are sequentially stacked.

20. (Original) A device according to claim 5, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

Claims 21-27 (Cancelled)

28. (Original) A semiconductor device comprising:
non-LOCOS insulating device isolation blocks for demarcating an element formation region on a semiconductor substrate, said non-LOCOS insulating device isolation block being formed by burying a first conductive film in a first insulating film;

second conductive films filled, with intermediary of second insulating films, between adjacent ones of said non-LOCOS insulating device isolation blocks on said semiconductor substrate, capacitively coupled to said first conductive film through a side surface portion of said first insulating film, and separated into an island shape in said element formation region; and

a third conductive film patterned into a strip shape on said second conductive film through a third insulating film and capacitively coupled to said second conductive film.

29. (Original) A device according to claim 28, wherein said non-LOCOS insulating device isolation blocks are patterned into a strip shape, and said third conductive film is formed to be substantially perpendicular to said non-LOCOS insulating device isolation blocks.

30. (Original) A device according to claim 28, wherein an upper surface of said second conductive film is substantially flush with upper surfaces of said non-LOCOS insulating device isolation blocks.

31. (Original) A device according to claim 28, wherein said device comprises a pair of impurity diffusion layers formed in surface regions of said semiconductor substrate on both sides of said second conductive film in said element formation region, and

a fourth conductive film patterned into a strip shape to be substantially perpendicular to said third conductive film; and

one of said impurity diffusion layers is electrically connected to said fourth conductive film.

32. (Original) A device according to claim 28, wherein said third conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said third conductive film.

33. (Original) A device according to claim 28, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

34. (Original) A semiconductor device comprising:

non-LOCOS insulating device isolation blocks for demarcating an element formation region on a semiconductor substrate, said non-LOCOS insulating device isolation block being formed by burying a first conductive film in a first insulating film;

a second conductive film filled, with intermediary of second insulating films, between adjacent ones of said non-LOCOS insulating device isolation blocks on said semiconductor substrate, and capacitively coupled to said first conductive film through a side surface portion of said first insulating film.

35. (Original) A device according to claim 34, wherein said second conductive film is a floating gate separated into an island shape in said element formation region.

36. (Original) A device according to claim 34, further comprising a third conductive film patterned into a strip shape on said second conductive film with intermediary of a third insulating film and capacitively coupled to said second conductive film.

37. (Original) A device according to claim 34, wherein said non-LOCOS insulating device isolation blocks are patterned into a strip shape, and said third conductive film is formed to be substantially perpendicular to said non-LOCOS insulating device isolation blocks.

38. (Original) A device according to claim 34, wherein an upper surface of said second conductive film is substantially flush with upper surfaces of said non-LOCOS insulating device isolation blocks.

39. (Original) A device according to claim 34, wherein said device comprises a pair of impurity diffusion layers formed in surface regions of said semiconductor substrate on both sides of said second conductive film in said element formation region, and

a fourth conductive film patterned into a strip shape to be substantially perpendicular to said third conductive film; and

one of said impurity diffusion layers is electrically connected to said fourth conductive film.

40. (Original) A device according to claim 34, wherein said third conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said third conductive film.

41. (Original) A device according to claim 34, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

42. (Original) A semiconductor device comprising:

a semiconductor region where a pair of first diffusion layers of a predetermined conductivity type are formed on surface regions;

a first layer having a conductive film patterned on said semiconductor region with a first insulating film intervened, said first diffusion layers being formed on left and right sides of said conductive film, a second insulating film formed on an upper surface of said conductive film, a third insulating film covering side surfaces of said conductive film and said second insulating film and planarized such that an upper surface of said third insulating film and an upper surface of said second insulating film are formed on substantially the same plane; and

a second layer patterned on said third insulating film including said upper surface of said second insulating film, in which a pair of second diffusion layers of a predetermined conductivity type are formed in regions on both sides of said second insulating film such that a

region between said second diffusion layers opposes said conductive film through said second insulating film.

43. (Original) A device according to claim 42, wherein said third insulating film is planarized by chemical mechanical polishing.

44. (Original) A device according to claim 42, wherein said semiconductor region is a region on a semiconductor substrate.

45. (Original) A device according to claim 42, wherein said first and second diffusion layers are of conductivity types different from each other.

46. (Original) A device according to claim 42, wherein said first and second diffusion layers have the same conductivity type.

47. (Original) A device according to claim 42, further comprising a step structure on said semiconductor region, said step structure being formed in said third insulating film and planarized such that an upper surface of said step structure and said upper surface of said third insulating film are on substantially the same plane.

48. (Original) A device according to claim 42, wherein a step structure is formed on said semiconductor region, and an upper portion of another conductive film having said second insulating film on an upper surface is patterned on said step structure, and

said step structure and said another conductive film are formed in said third insulating film and planarized such that said upper surface of said second insulating film and said upper surface of said third insulating film are on substantially the same plane.

49. (Original) A device according to claim 48, wherein said upper surface of said third insulating film is planarized by chemical mechanical polishing.

50. (Original) A device according to claim 48, wherein said step structure is a non-LOCOS insulating device isolation block for demarcating an element formation region as a conductive film formation portion on said semiconductor region.

51. (Original) A device according to claim 42, further comprising a silicide film consisting of a refractory metal on a surface of said first insulating film.

Claims 52-62 (Cancelled)

63. (Original) A semiconductor device comprising:

a first insulating film filled in a groove formed in a semiconductor substrate;

first conductive films patterned, with intermediary of a second insulating film, on at least a first insulating film nonformation region of said semiconductor substrate over said first insulating film nonformation region and said first insulating film;

a third insulating film covering said first conductive film;

a pair of diffusion layers formed in surface regions of said semiconductor substrate on both sides of said first conductive film; and

a second conductive film filled, with intermediary of said third insulating film, between adjacent ones of said first conductive films and connected to said diffusion layer,

wherein upper surfaces of said first conductive films are planarized across said nonformation region and said first insulating film on substantially the same plane, and an upper surface of said third insulating film and an upper surface of said second conductive film are planarized on substantially the same plane.

64. (Original) A device according to claim 63, wherein said upper surfaces of said first conductive films and said second conductive film are planarized by chemical mechanical polishing.

65. (Original) A device according to claim 63, wherein said first and second conductive films are formed of silicon films.

66. (Original) A device according to claim 63, wherein said first insulating film filled in the groove is a non-LOCOS insulating device isolation block for demarcating an element active region on said semiconductor substrate.

67. (Original) A device according to claim 63, further comprising a diffusion prevention film covering at least an inner wall surface of the groove, and wherein said first insulating film is filled in the groove with intermediary of said diffusion prevention film.

68. (Original) A semiconductor device in which a transistor having a gate, a source, and a drain is formed in an element active region on a semiconductor substrate, comprising:

a non-LOCOS insulating device isolation block formed by filling a first insulating film in a groove formed in said semiconductor substrate to demarcate said element active region on said semiconductor substrate;

a second insulating film covering said gate; and

a leading-out electrode filled, with intermediary of said second insulating film, between adjacent ones of said gates, having an upper surface which is planarized to be on substantially the same plane as that of an upper surface of said second insulating film, and connected to said source or drain.

69. (Original) A device according to claim 68, wherein said leading-out electrode is planarized by chemical mechanical polishing.

70. (Original) A device according to claim 68, wherein said gate is formed across said element active region and said first insulating film.

71. (Original) A device according to claim 68, wherein said leading-out electrode is planarized by chemical mechanical polishing.

72. (Original) A device according to claim 68, wherein said gate and said leading-out electrode are formed of silicon films.

73. (Original) A device according to claim 68, further comprising a diffusion prevention film covering at least an inner wall surface of the groove, and wherein said first insulating film is filled in the groove with intermediary of said diffusion prevention film.

74. (Original) A device according to claim 68, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

75. (Original) A semiconductor device in which first and second transistors are stacked,

wherein said first transistor has a first gate patterned on a semiconductor substrate with intermediary of a first gate insulating film, and first source and drain formed in surface regions of said semiconductor substrate on both sides of said first gate,

an insulating interlayer having an upper surface is formed to cover said first gate, and

said second transistor includes a conductive film patterned on said insulating interlayer, and has a second gate patterned on said conductive film through a second gate insulating film and second source and drain formed in said conductive film on both sides of said second gate.

76. (Original) A device according to claim 75, wherein said insulating interlayer is planarized by chemical mechanical polishing.

77. (Original) A device according to claim 75, wherein said first source and said first drain have a conductivity type different from that of said second source and said second drain.

78. (Original) A device according to claim 75, wherein said first source and said first drain have the same conductivity type as that of said second source and said second drain.

79. (Original) A device according to claim 75, wherein said conductive film is formed of a silicon film.

80. (Original) A device according to claim 75, further comprising a silicide layer of a refractory metal formed on surfaces of said first and second gates.

81. (Original) A device according to claim 75, further comprising a step structure formed on said semiconductor substrate,

said step structure being formed in said insulating interlayer and planarized such that an upper surface of said step structure and an upper surface of said insulating interlayer are on substantially the same plane.

82. (Original) A device according to claim 81, wherein said insulating interlayer is planarized by chemical mechanical polishing.

83. (Original) A device according to claim 75, wherein a step structure is formed on said semiconductor substrate, an upper portion of another first gate is patterned on said step structure, and

said step structure and said another first gate are formed in said insulating interlayer and planarized such that an upper surface of said another first gate and said upper surface of said insulating interlayer are on substantially the same plane.

84. (Original) A device according to claim 83, wherein said insulating interlayer is planarized by chemical mechanical polishing.

85. (Original) A device according to claim 83, wherein said step structure is a non-LOCOS insulating device isolation block for demarcating an element active region where said first transistor is formed on said semiconductor substrate.

86. (Original) A device according to claim 75, further comprising a first side wall formed on a side surface of said first gate of said first transistor, and

wherein each of said first source and drain is constituted by a first lightly doped diffusion layer formed in said semiconductor substrate near a lower portion of said first side wall, and a first heavily doped diffusion layer formed in said semiconductor substrate to be joined to said first lightly doped diffusion layer.

87. (Original) A device according to claim 75, further comprising a second side wall formed on a side surface of said second gate of said second transistor, and

wherein each of said second source and drain is constituted by a second lightly doped diffusion layer formed in said conductive film near a lower portion of said second side wall, and

a second heavily doped diffusion layer formed in said conductive film to be joined to said second lightly doped diffusion layer.

88. (Original) A device according to claim 75, further comprising a cap insulating film formed on said first gate, and wherein said conductive film is formed on planarized surfaces of said insulating interlayer and said cap insulating film.

89. (Original) A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate and having an opening for exposing a part of a surface of said semiconductor substrate;

a lower electrode patterned on said insulating film to bury the opening and having a planarized upper surface;

an upper electrode patterned on said lower electrode with intermediary of a dielectric film and capacitively coupled to said lower electrode,

wherein another insulating film is formed to bury sides of said lower electrode, said dielectric film and said upper electrode, said another insulating film being planarized to have a top surface flushed with the top surface of said upper electrode.

90. (Original) A device according to claim 89, wherein said upper surfaces of said lower electrode and said insulating film is planarized by chemical mechanical polishing.

Claims 91-202 (Cancelled)

203. (Original) A semiconductor device having a transistor with a gate, a source, and a drain formed in an element active region demarcated by element isolation structures on a semiconductor substrate, comprising:

at least two gate structures each including said gate covered with insulating film and formed on said element active region to extend over said element isolation structures; and

a leading-out electrode filled between adjacent ones of said gate structures,

wherein upper surfaces of said gate structures are planarized at substantially the same level over said element isolation structures and said element active region, and upper surfaces of said insulating films and an upper surface of said leading-out electrode are planarized at substantially the same level.

204. (Original) A device according to claim 203, wherein said upper surfaces of said gates, said upper surfaces of said insulating films, and said upper surface of said leading-out electrode are planarized by chemical mechanical polishing.

205. (Original) A device according to claim 203, wherein said element isolation structure is a field shield element isolation structure which has a shield plate electrode patterned with intermediary of a shield gate insulating film and a cap insulating film covering said shield plate electrode and fixes a portion of said semiconductor substrate positioned below said shield plate electrode to a predetermined potential.

206. (Original) A device according to claim 203, wherein upper surfaces of cap insulating films formed on said gates and the upper surface of said leading-out electrode are planarized at substantially the same level.

207. (Original) A device according to claim 203, wherein said element isolation structure is a trench type element isolation structure.

208. (Original) A semiconductor device comprising:

a first step structure portion made of a silicon film formed at a predetermined level from a surface of a semiconductor substrate;

a second step structure portions respectively formed on said first step structure portion and on said semiconductor substrate,- said second step structure portion on said semiconductor substrate serving as a field oxide film for demarcating element active regions; and

conductive films patterned in said element active region to span over at least said second step structure portion on said semiconductor substrate,

wherein upper surfaces of said conductive films are planarized at substantially the same level.

209. (Original) A device according to claim 208, wherein said upper surfaces of said conductive films are planarized by a chemical mechanical polishing process.

210. (Original) A device according to claim 208, wherein each of said conductive films constitutes an element of gate structure of a transistor.

211. (Original) A device according to claim 208, wherein said first step structure portion is formed on a scribing line region of said semiconductor substrate.